REMARKS

Claims 1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42 are pending.

Claims 12 and 20 stand rejected under 35 U.S.C. § 101 as lacking specific or a well established utility. Applicant respectfully traverses the rejection.

Claim 12 recites an apparatus for testing a match line of a memory device and claim 20 recites a memory device for testing CAM devices. The claimed invention is used for testing content addressable memory devices (¶ [0016]) and as such, has a specific and well established utility.

Claims 12 and 20 stand rejected under 35 U.S.C. § 112, first paragraph. Applicant respectfully traverses the rejection.

Claim 12 recites an apparatus for testing a match line of a memory device comprising, in part, "said circuit determining a status of the match line under test based on a result of a search operation and a signal on the match line under test after confirming proper operation of a control line used to generate a signal on the word line." Claim 20 recites a memory device comprising, in part, "said enabling circuitry enabling said match line in response to a signal on said word line, said enabling circuitry enabling the match line after confirming proper operation of a control line used to generate the signal on the word line."

The Office Action contends that the limitation "a control line used to generate the signal on the word line" is not supported by the specification or drawings. Additionally, the Office Action contends that the claims fail to satisfy the enablement requirement because of lack of utility. (Office Action, p.2). Applicant respectfully

disagrees with these contentions. As indicated earlier, the claimed invention has a specific utility. The limitation "a control line used to generate the signal on the word line" has support in the specification, i.e., the specification describes a "[r]ead/write decode logic block 440 [that] outputs the WL signal on word line 132," (¶ [0046]), and a "read/write decode logic block 440 [that] decodes the address and provides a pulse on the CAM word line 132 indicated by the address in the step in box 625." (¶ [0056]). Therefore, Applicant respectfully requests that the rejection of claims 12 and 20 be withdrawn and the claims allowed.

Claims 1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 7,002,823 ("Ichiriu") in view of U.S. Patent No. 6,944,039 ("Nataraj"). Applicant respectfully traverses the rejection.

Claim 1 recites a method for testing a memory device comprising, in part, "resetting all match lines of said memory device; confirming proper operation of a control line used to enable output from a match line under test; enabling output from the match line under test; decoding an address of a selected memory storage location corresponding to said match line under test."

Ichiriu is directed to error detection within content addressable memory devices having a simultaneous write and compare function. (Ichiriu, Abstract; col. 1, lines 18-20). The Ichiriu device includes a CAM array 101, address circuit 103, instruction decoder 105, error detector 107, flag circuit 112, priority encoder 114, comparand register 115 and read/write circuit 161. (Ichiriu, col. 3, lines 30-35). During a compare operation, any match between the comparand and a valid CAM word that results in a match signal is output to the priority encoder 114 and the flag circuit 112 via the corresponding match line 182.

(Ichiriu, col. 3, line 64 to col. 4, line 6). Ichiriu merely discloses testing for parity errors of CAM cells and error correction when errors are found. (Ichiriu, col. 4, lines 15-34; col. 5, lines 1-15; col. 7, lines 41-45).

Ichiriu does not disclose or suggest testing physical match lines for errors, i.e., Ichiriu does not have a "match line under test" because Ichiriu is only concerned with performing "simultaneous write and compare" functions and performing parity testing and error correction on the CAM cells themselves. The Office Action does not respond to Applicant's above-mentioned arguments made in the Amendment filed on September 11, 2006. (Office Action, p.15). Further, the Office Action concedes that Ichiriu does not disclose or suggest "confirming proper operation of a control line used to enable output from a match line under test; enabling output from the match line under test." (Office Action, p.4).

The Office Action relies on Nataraj to only teach "confirming proper operation of a control line used to enable output from a match line under test; enabling output from the match line under test." Nataraj is directed to content addressable memory with mode-selectable match detect timing. (Nataraj, Abstract). The Nataraj device includes a CAM array 201, comparand register 207, compare line driver 209, instruction decoder 205, read/write circuit 211, match latch circuit 203 and priority encoder/flag logic circuit 215. (Nataraj, col. 5, lines 15-20). The match latch circuit 203 includes an AND gate having a first input coupled to receive a detect signal and a second input coupled to receive a match line 241 and outputting a corresponding match signal 251 to the priority encoder/flag logic circuit 215. (Nataraj, col. 6, lines 42-53). But the AND gate in the Nataraj device does not use a match line reset value and does not cure the deficiencies of Ichiriu.

Because the references, individually or in combination, do not disclose, teach or suggest all of the limitations of claim 1, Applicant respectfully requests the rejection of independent claim 1 and dependent claims 2-7 be withdrawn and the claims allowed.

Claim 4 depends from claim 1 and further recites "said resetting and said decoding acts occur on the rising edge of a clock signal."

The Office Action contends that Ichiriu teaches this limitation. (Office Action, p.5). Applicant respectfully disagrees. The cited portions of Ichiriu only disclose that the instruction decoder 105 transitions from state to state in response to transitions of a clock signal 104. (Ichiriu, col. 4, lines 57-61). Further, Ichiriu does not disclose or suggest when the transition occurs due to a change in the clock signal. Particularly, Ichiriu does not disclose or suggest "said resetting and said decoding acts occur on the rising edge of a clock signal." (emphasis added). Therefore, Applicant respectfully submits that the rejection of claim 4 be withdrawn and the claim allowed.

Claim 5 depends from claim 1 and further recites "said loading acts occur on the rising edge of a clock signal."

The Office Action contends that Ichiriu teaches this limitation. (Office Action, p.5). Applicant respectfully disagrees. The cited portions of Ichiriu only disclose that the instruction decoder 105 transitions from state to state in response to transitions of a clock signal 104. (Ichiriu, col. 4, lines 57-61). Ichiriu does not disclose or suggest when the transition occurs due to a change in the clock signal. Particularly, Ichiriu does not disclose or suggest "said loading acts occur on the rising edge of a clock signal." (emphasis

added). Therefore, Applicant respectfully submits that the rejection of claim 5 be withdrawn and the claim allowed.

Claim 8 recites a method of testing a memory device comprising, in part, "confirming proper operation of a control line used to enable output from said match line of a set of memory cells being tested; enabling said match line of the set of memory cells being tested and disabling match lines of other sets of memory cells."

Both Ichiriu and Nataraj fail to disclose, teach or suggest at least these limitations of claim 8. Therefore, Applicant respectfully requests the rejection of independent claim 8 and dependent claims 9-10 be withdrawn and the claims allowed.

Claims 12 recites an apparatus for testing a match line of a memory device comprising, in part, "a memory storage location corresponding to a match line under test, said match line under test further having a corresponding word line; a comparator coupled to at least one search line per CAM memory cell of said memory storage location; and a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of the match line under test based on a result of a search operation and a signal on the match line under test after confirming proper operation of a control line used to generate a signal on the word line."

Ichiriu does not disclose or suggest testing physical match lines for errors, i.e., Ichiriu does not have a "match line under test" because Ichiriu is only concerned with performing "simultaneous write and compare" functions and performing parity testing and error correction on the CAM cells themselves. Further, Ichiriu does not teach or suggest confirming proper operation of a control line used to generate a signal on a word

line or a circuit coupled to match line under test, a word line and a test mode match line reset signal. Nataraj does not cure the deficiencies of Ichiriu because the AND gate in the Nataraj device does not use a match line reset signal. Because the references do not disclose, teach or suggest all of the limitations of claim 12, independent claim 12 and dependent claims 13 and 14 are allowable.

Claim 17 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and enabling circuitry that enables a match line to provide said match signal as an output when said set of memory cells is being tested, said enabling circuitry enabling the match line after confirming proper operation of a control line."

The Office Action concedes that Ichiriu does not disclose or suggest "confirming proper operation of a control line used to enable output from a match line under test; enabling output from the match line under test," as recited in claim 1. (Office Action, p.4). These limitations are similar to the limitations of claim 17. Thus, Ichiriu does not disclose or suggest "enabling circuitry that enables a match line to provide said match signal as an output . . . said enabling circuitry enabling the match line after confirming proper operation of a control line."

Further, the Office Action concedes that Ichiriu does not disclose or suggest "enabling circuitry enabling the match line after confirming proper operation of a control line." (Office Action, p.10). Accordingly, it relies on Nataraj to teach this limitation. The Office Action contends that a person of ordinary skill in the art would have combined the Ichiriu's priority encoder and Nataraj's flag logic circuit comprising inputs of match

signals and outputs of match addresses and match flag. (Office Action, p.10). However, the AND gate in the Nataraj device does not use a match line reset signal. Accordingly, Applicant respectfully submits that independent claim 17 and dependent claims 19 are allowable over the cited combination.

Claim 20 recites "for each set of memory cells, enabling circuitry that enables a match line to provide said match signal as an output when said set of memory cells is being tested; for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to a signal on said word line, said enabling circuitry enabling the match line after confirming proper operation of a control line used to generate the signal on the word line; and control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled."

The Office Action concedes that Ichiriu does not disclose or suggest "confirming proper operation of a control line used to enable output from a match line under test; enabling output from the match line under test," as recited in claim 1. (Office Action, p.4). These limitations are similar to the limitations of claim 20. Thus, Ichiriu does not disclose or suggest "said enabling circuitry enabling said match line in response to a signal on said word line, said enabling circuitry enabling the match line after confirming proper operation of a control line used to generate the signal on the word line."

Further, the Office Action concedes that Ichiriu does not disclose or suggest "enabling circuitry enabling the match line after confirming proper operation of a control line." (Office Action, p.10); it relies on Nataraj to teach this limitation. Nataraj does not cure the deficiencies of Ichiriu because the AND gate in the Nataraj device does not use a

match line reset signal. Therefore, Applicant respectfully submits that independent claim 20 and dependent claims 21 and 22 are allowable over the cited combination.

Claim 23 recites a "circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of a write enable signal used to generate a signal on the word line and determining a status of the match line under test based on a result of a search operation and a signal on the match line under test."

Ichiriu does not disclose or suggest testing physical match lines for errors, i.e., Ichiriu does not have a "match line under test" because Ichiriu is only concerned with performing "simultaneous write and compare" functions and performing parity testing and error correction on the CAM cells themselves. Further, Ichiriu does not disclose or suggest a circuit coupled to a match line under test, a word line and a test mode match line reset signal. Nataraj does not cure the deficiencies of Ichiriu because the AND gate in the Nataraj device does not use a match line reset signal. Accordingly, Applicant respectfully submits that claim 23 is allowable over the cited combination.

Claim 30 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested."

Ichiriu does not disclose or suggest "enable output from a match line under test." The Office Action concedes that Ichiriu does not teach "the enabling circuitry for

enabling a match line." (Office Action, p.12). The Office Action contends that Nataraj teaches a match latch circuit that outputs a logic-level match signal in high or low state according to whether the signal level of the corresponding match line is above or below a threshold. Nataraj, however, does not cure the deficiencies of Ichiriu because the AND gate in the Nataraj device does not use a match line reset signal. Particularly, the references fail to disclose or suggest "enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested." Therefore, Applicant respectfully submits that independent claim 30 and dependent claim 32 are allowable over the cited combination.

Claim 33 recites "for each set of memory cells, comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; for each set of memory cells, enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested; for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said single match line in response to a signal on said word line; and control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled."

In rejecting claim 30, the Office Action concedes that Ichiriu does not teach "the enabling circuitry for enabling a match line." (Office Action, p.12). The Office Action contends that claim 33 is similar to claim 30 with the additional recited control circuitry for resetting the enabling circuitry. (Office Action, p.13). The Office Action contends that Nataraj teaches a match latch circuit that outputs a logic-level match signal in high or low

state according to whether the signal level of the corresponding match line is above or below a threshold. (Office Action, pp.13-14). But the match latch circuit 203 of the Nataraj device includes an AND gate having a first input coupled to receive a detect signal and a second input coupled to receive a match line 241 and outputting a corresponding match signal 251 to the priority encoder/flag logic circuit 215. (Nataraj, col. 6, lines 42-53). The AND gate does not use a match line reset signal and does not cure the deficiencies of Ichiriu. Particularly, the references fail to disclose or suggest "for each set of memory cells, enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested; for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said single match line in response to a signal on said word line." Accordingly, Applicant respectfully submits that independent claim 33 and dependent claims 34 and 35 are allowable over the cited combination.

Claim 36 recites "comparison circuitry that that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested."

The Office Action contends that claims 36 and 38 are "similar to claims 30 and 32 except that a router is being recited" and that Ichiriu teaches a routing device. (Office Action, p.14). As mentioned above, responsive to rejection of claim 30, the references fail to disclose or suggest "enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested." Accordingly,

Applicant respectfully submits that independent claim 36 and dependent claims 38, 40 and 41 are allowable over the cited combination.

Claim 39 recites "for each set of memory cells, comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; for each set of memory cells, enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested; for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said single match line in response to a signal on said word line; and control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled."

The Office Action contends that claim 39 is "similar to claim 33 except that a router is being recited" and that Ichiriu teaches a routing device. (Office Action, p.14). As mentioned above, responsive to rejection of claim 33, the references fail to disclose or suggest "for each set of memory cells, enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested; for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said single match line in response to a signal on said word line." Accordingly, Applicant respectfully submits that claim 39 is allowable over the cited combination.

Claim 42 recites "confirming proper operation of a control line used to enable output from said match line under test; enabling said match line under test; . . . loading

said selected memory storage location with a known data pattern; loading a comparand register with said known data pattern; performing a search operation, for the known data pattern in the comparand register, on said memory device; and outputting a result of said search operation; comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation."

The Office Action concedes that Ichiriu does not disclose or suggest "confirming proper operation of a control line used to enable output from a match line under test; enabling output from the match line under test." (Office Action, p.4). But the Office Action contradicts, in rejecting claim 42, by stating that claim 42 "is similar to claims 1 and 12 with additional processing system having a processor." (Office Action, p.15). Because the Office Action failed to state proper grounds for rejecting claim 42 and the references do not teach or suggest all of the limitations of claim 42, Applicant respectfully submits that claim 42 is allowable.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Gianni Minutoli
Registration No.: 41,198
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant